Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A data transfer control device for transferring data among a plurality of nodes that are connected to a bus, said data transfer control device comprising:

a management circuit which manages an interface with a random accessible storage memory so that control information of a packet is written by a first upper layer into a control information area of said random accessible storage memory and data of said packet corresponding to said control information is written by a second upper layer into a data area different from said control information area of said random accessible storage memory, said randomly accessible storage memory being divided into said control information area and said data area;

a packet assembly circuit which reads ~~means for reading~~ control information of said ~~a~~ packet from said ~~a~~ control information area ~~of a randomly accessible storage means~~ and reads ~~reading~~ data of said packet corresponding to said control information from said ~~a~~ data area; ~~area of said randomly accessible storage means, said randomly accessible storage means being divided into said control information area for control information that is written thereto by an upper layer and said data area for data that is written thereto by an upper layer;~~ and

a link circuit which provides ~~means for providing~~ a service for transferring said read-out packet to each of nodes.

2. (Currently Amended) The data transfer control device as defined in claim 1,

wherein said packet assembly circuit ~~means~~ obtains a data pointer indicating an address of data that is to be read from said data area, from control information that has

been read from said control information area, and uses the obtained data pointer to read data from said data area.

3. (Currently Amended) The data transfer control device as defined in claim 2, wherein said packet assembly circuit ~~means~~ utilizes a period of time during which said link circuit ~~means~~ is creating error-checking information for said control information of said packet, to obtain a data pointer from control information.

4. (Currently Amended) The data transfer control device as defined in claim 1, wherein said packet assembly circuit ~~means~~ updates a control information pointer indicating an address of control information to be read from said control information area when it is determined based on packet format identification information included in said control information of said packet that said control information of said packet is read, and updates a data pointer indicating an address of data that is to be read from said data area when it is determined based on said packet format identification information that said data of said packet is read.

5. (Currently Amended) The data transfer control device as defined in claim 2, wherein said packet assembly circuit ~~means~~ updates a control information pointer indicating an address of control information to be read from said control information area when it is determined based on packet format identification information included in said control information of said packet that said control information of said packet is read, and updates a data pointer indicating an address of data that is to be read from said data area when it is determined based on said packet format identification information that said data of said packet is read.

6. (Currently Amended) The data transfer control device as defined in claim 3, wherein said packet assembly circuit ~~means~~ updates a control information pointer indicating an address of control information to be read from said control information

area when it is determined based on packet format identification information included in said control information of said packet that said control information of said packet is read, and updates a data pointer indicating an address of data that is to be read from said data area when it is determined based on said packet format identification information that said data of said packet is read.

7. (Currently Amended) The data transfer control device as defined in claim 1, further comprising:

control information creation section which creates ~~means for creating~~ control information and writes ~~writing~~ said control information to said control information area, during processing for fetching data to said data area; and

transmission start section which instructs ~~means for instructing~~ a start of transmission of a packet, on condition that both data fetch processing and control information write processing have been completed.

8. (Currently Amended) The data transfer control device as defined in claim 2, further comprising:

control information creation section which creates ~~means for creating~~ control information and writes ~~writing~~ said control information to said control information area, during processing for fetching data to said data area; and

transmission start section which instructs ~~means for instructing~~ a start of transmission of a packet, on condition that both data fetch processing and control information write processing have been completed.

9. (Currently Amended) The data transfer control device as defined in claim 3, further comprising:

control information creation section which creates ~~means for creating~~ control information and writes ~~writing~~ said control information to said control information area, during processing for fetching data to said data area; and

transmission start section which instructs ~~means for instructing~~ a start of transmission of a packet, on condition that both data fetch processing and control information write processing have been completed.

10. (Currently Amended) The data transfer control device as defined in claim 4, further comprising:

control information creation section which creates ~~means for creating~~ control information and writes ~~writing~~ said control information to said control information area, during processing for fetching data to said data area; and

transmission start section which instructs ~~means for instructing~~ a start of transmission of a packet, on condition that both data fetch processing and control information write processing have been completed.

11.-24. (Cancelled)

25. (Currently Amended) The data transfer control device as defined in claim 1, said data transfer control device further comprising:

a first bus connected to a next-stage application;

a second bus for controlling said data transfer control device;

a third bus connected electrically to a physical-layer device;

a fourth bus connected electrically to said storage memory ~~means~~; and

an arbitration circuit which performs ~~means for performing~~ arbitration for establishing a data path between any one of said first, second, and third buses and said fourth bus.

26.-28. (Cancelled)

29. (Original) The data transfer control device as defined in claim 1, wherein data transfer is performed in accordance with the IEEE 1394 standard.

30.-32. (Cancelled)

33. (Currently Amended) Electronic equipment comprising: a data transfer control device as defined in ~~any of claims 1 to 32~~claim 1;

a device for performing given processing on data that has been received from another node via said data transfer control device and said bus; and

a device for outputting or storing data that has been subjected to said processing.

34. (Withdrawn - Currently Amended) Electronic equipment comprising: a data transfer control device as defined in ~~any of claims 1 to 32~~claim 1;

a device for performing given processing on data that is to be sent to another node via said data transfer control device and said bus; and

a device for fetching data to be subjected to said processing.

35. (New) The data transfer control device as defined in claim 1, further comprising a first-in first-out memory that is provided between said random accessible storage memory and said link circuit, and stores said packet read by said packet assembly circuit.